REMARKS/ARGUMENTS

This is intended as a full and complete response to the Office Action dated December 1, 2004, having a shortened statutory period for response set to expire on March 1, 2005. Applicants request petition for a two month extension of time under 37 CFR Paragraph 1.136(a).

Claims 53-54, 56-70 stand rejected under 35 U.S.C 103(a) as being unpatentable over Baxter et al, U.S. Patent No. 6,026,461 (Baxter), in view of Nishtala et al U.S. Patent No. 5,581,729 (Nishtala). Please enter the following amendments and reconsider the claims pending in the application for reasons discussed below. Applicants have amended claims 53, 56-70 to more clearly recite the invention. Claim 54 is cancelled without prejudice. New claims 71-74 have been added. Applicants aver that no new matter has been introduced in this response.

35 U.S.C 103(a) Rejection

Claim 53

Claim 53 stand rejected under 35 U.S.C 103(a) as being unpatentable over Baxter in view of Nishtala. The Applicants respectfully assert that claim 53 is allowable over those references.

For example, claim 53 recites in part "receiving the plurality of memory access requests in an initial queue", and "reordering the memory access requests according to a predetermined precedence order defined by a set of rules, *without regard to the state of [a] plurality of processors* (emphasis added)." Baxter and Nishtala, neither alone nor in combination, teach, show or suggest at least these elements.

For example, Baxter teaches a cache based system that maintains a full-map directory structure cache coherency protocol. Baxter teaches a three level priority scheme which work in conjunction with an arbitration service and a "shuffle code". As stated by the Examiner the "shuffle code is used to prioritize the memory requests based on "fairness"". The "shuffle code" as taught by Baxter refers to a 3-bit randomization code initiated by a counter circuit to

ensure the all of the processors sending requests do not "unfairly" take up the existing bus request bandwidth. Baxter teaches that the request be identified with a particular processor (i.e., bus requestor). Baxter does not teach reordering the memory access requests according to a predetermined precedence order defined by a set of rules without regard to the state of the plurality of processors. On the contrary, the identification is used to allow each processor to know the status of the request relative to the status of other request by other processors on the bus. Therefore, Baxter *teaches the input queue state of the processor requesting bus access and a random code are used to facilitate the arbitration of access to the system bus* (emphasis added) (See Abstract, col. 4 lines 65-68, col. 5, lines 52-68, col. 6, lines 1-68, col. 22 line 65 though col. 23 line 18, col. 71 line 37 though col. 72 line 54).

Nishtala teaches a coherent read and write back transaction processing having a plurality of parallel processors. Nishtala teaches an interconnect module and a system controller connected to the parallel processors and to a snoop bus. Similar to Baxter, Nishtala does not teach reordering the memory access requests according to a predetermined precedence order defined by a set of rules without regard to the state of the plurality of processors. On the contrary, the system controller uses a set of duplicate cache tags (Dtags) to *associate the memory transactions with a particular processor* (emphasis added). For example, the processors have a master class that allow for simultaneous launching of read and write transactions. (See Abstract, FIG. 1-2, col. 2, lines 4-68, col. 10 lines 33-36, col. 77 line 44 through col. 78 line 53).

Therefore, since claim 53 includes at least one element not disclosed or suggested by Baxter or Nishtala, the Applicants submit that the rejection has been obviated and respectfully request the Examiner to withdraw the rejection.

Claim 56

Claims 56 stand rejected under 35 U.S.C 103(a) as being unpatentable over Baxter in view of Nishtala. The Applicants respectfully assert that claim 56 is allowable over those references.

For example, claim 56 partially recites "receiving the plurality of memory access requests in an initial queue," and "reordering the memory access requests according to a predetermined precedence order defined by a set of rules, without regard to the state of the plurality of processors." Baxter and Nishtala, neither alone nor in combination, teach, show or suggest at least these elements.

Similar to the above arguments, Baxter and Nishtala do not teach reordering the memory access requests according to a predetermined precedence order defined by a set of rules, without regard to the state of the plurality of processors. On the contrary, as with the above argument, Baxter *teaches the input queue state of the processor requesting bus access and a random code are used to facilitate the arbitration of access to the system bus* and Nishtala *teaches associating the memory transactions with a particular processor* (emphasis added).

Therefore, since claim 56 includes at least one element not disclosed or suggested by Baxter or Nishtala, the Applicants submit that the rejection has been obviated and respectfully request the Examiner to withdraw the rejection.

Claims 57-61

Claims 57-61 which depend from claim 56, are allowable for at least the reasons discussed in relation to claim 56, as well as the additional limitations they recite.

Claim 62

Claim 62 stands rejected under 35 U.S.C 103(a) as being unpatentable over Baxter in view of Nishtala. The Applicants respectfully assert that claim 62 is allowable over those references.

For example, claim 62 partially recites "a reordering unit configured to reorder [a] first order of the plurality of memory access requests into a second order, *without regard to a status of the plurality of the processors* (emphasis added)." Baxter and Nishtala, neither alone nor in combination, teach, show or suggest at least these elements.

Similar to the arguments already stated above, Baxter and Nishtala do not teach a reordering unit configured to reorder the first order of the plurality of memory access requests into a second order without regard to a status of the plurality of the processor. On the contrary, as with the above arguments, Baxter *teaches the input queue state of the processor requesting bus access and a random code are used to facilitate the arbitration of access to the system bus* and Nishtala *teaches associating the memory transactions with a particular processor* (emphasis added).

Therefore, since claim 62 includes at least one element not disclosed or suggested by Baxter or Nishtala, the Applicants submit that the rejection has been obviated and respectfully request the Examiner to withdraw the rejection.

Claim 63

Claim 63 which depends from claim 62, is allowable for at least the reasons discussed in relation to claim 62, as well as the additional limitations it recites.

Claim 64

Claim 64 stands rejected under 35 U.S.C 103(a) as being unpatentable over Baxter in view of Nishtala. The Applicants respectfully assert that claim 64 is allowable over those references.

For example, claim 64 partially recites "storing the plurality of memory access requests in a receiving order ", " an ordering module for determining the execution order from [a] receiving order," and "the ordering module configured to reorder the receiving order into the execution order...*regardless of the state of the plurality of processors* (emphasis added)." Baxter and Nishtala, neither alone nor in combination, teach, show or suggest at least these elements.

Similar to the arguments already stated above, Baxter and Nishtala do not teach ordering module configured to reorder the receiving order into the execution order regardless of the state of the plurality of processors. On the contrary, as with the above argument, Baxter *teaches the input queue state of the processor requesting bus access and a random code are used to facilitate the arbitration of access to the system bus* and Nishtala *teaches associating the memory transactions with a particular processor* (emphasis added).

Therefore, since claim 64 includes at least one element not disclosed or suggested by Baxter or Nishtala, the Applicants submit that the rejection has been obviated and respectfully request the Examiner to withdraw the rejection.

Claims 65-67

Claims 65-67 which depend from claim 64, are allowable for at least the reasons discussed in relation to claim 64, as well as the additional limitations they recite.

Claim 68

Claim 68 stands rejected under 35 U.S.C 103(a) as being unpatentable over Baxter in view of Nishtala. The Applicants respectfully assert that claim 68 is allowable over those references.

For example, claim 68 partially recites "reordering [an] initial order of [a] plurality of memory access requests with respect to [an] execution preference, *where the plurality of processors are not aware of the reordering process* (emphasis added)." Baxter and Nishtala, neither alone nor in combination, teach, show or suggest at least these elements.

Similarly to the above arguments, Baxter and Nishtala do not teach reordering an initial order of a plurality of memory access requests with respect to an execution preference, where the plurality of processors are not aware of the reordering process. On the contrary, as with the above argument, Baxter *teaches the input queue state of the processor requesting bus access and a random code are used to facilitate the arbitration of access to the system bus* and Nishtala *teaches associating the memory transactions with a particular processor* (emphasis added).

Therefore, since claim 68 includes at least one element not disclosed or suggested by Baxter or Nishtala, the Applicants submit that the rejection has been obviated and respectfully request the Examiner to withdraw the rejection.

Claim 69

Claim 69 stands rejected under 35 U.S.C 103(a) as being unpatentable over Baxter in view of Nishtala. The Applicants respectfully assert that claim 69 is allowable over those references.

For example, claim 69 partially recites " reordering [a] plurality of memory access requests *without regard to the status of [a] plurality of processors.* (emphasis added)" Baxter and Nishtala, neither alone nor in combination, teach, show or suggest at least these elements.

Similarly to the above arguments, Baxter and Nishtala do not teach reordering an initial order of a plurality of memory access requests with respect to an execution preference, where the plurality of processors are not aware of the reordering process. On the contrary, as with the above argument, Baxter *teaches the input queue state of the processor requesting bus access and a random code are used to facilitate the arbitration of access to the system bus* and Nishtala *teaches associating the memory transactions with a particular processor* (emphasis added).

Therefore, since claim 69 includes at least one element not disclosed or suggested by Baxter or Nishtala, the Applicants submit that the rejection has been obviated and respectfully request the Examiner to withdraw the rejection.

Claim 70

Claim 70 which depend from claim 69, is allowable for at least the reasons discussed in relation to claim 69, as well as the additional limitations it recites.

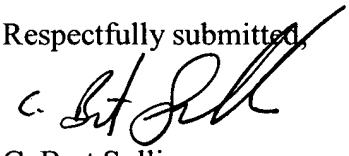
CONCLUSION

The prior art made of record is noted. However, it is believed that the secondary references are no more pertinent to the Applicants' disclosure than the primary references cited in the office action. Therefore, it is believed that a detailed discussion of the secondary references is not deemed necessary for a full and complete response to this office action.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (415) 576-0200.

Respectfully submitted,



C. Bart Sullivan
Reg. No. 41,516

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
Attachments
CBS:fcr
60481673 v1